

REMARKS

Claims 1-11 are pending in this application, of which claims 1-3, 7 and 8 are withdrawn from consideration. Claims 4, 6 and 9 have been amended. Claim 11 has been newly added. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment, which is captioned "Version with Markings to Show Changes Made."

Rejections under 35 USC §112, Second Paragraph

Claim 6 is rejected under 35 USC §112, first paragraph, as containing subject matter which was not described in the specification.

Claim 6 has been amended to overcome the rejection.

Claim 10 is also rejected under 35 USC §112, first paragraph, as containing subject matter which was not described in the specification.

The Examiner alleges that "wherein a width of said second film along a gate length direction is approximately equal to a width of said third film along the gate length direction" is not described in the specification or shown in the figures.

The specification and the figures, however, do show the feature. Fig. 5 shows gate mask patterns 111a and 111b. Gate mask pattern 111b corresponds to the second film, and gate mask pattern 111a corresponds to the third film. As shown in Figs. 6C and 6D and related description in the specification, at page 16, gate mask patterns 111a and 111b are etched using the resist pattern of the same width of W13.

Also, the width of the second film along the gate length direction of claim 10 corresponds to the width W12 shown in Fig. 4B. The width of the third film along the gate length direction is equal to the width of the gate electrode 102 along the gate length direction as shown in Fig. 5. Namely, the width of the third film along the gate length direction corresponds to the width W11 shown in Fig. 4A. The width W12 is equal to the width W11 as described at lines 8-11 on page 14.

Claims 9-10 are rejected under 35 USC §112, second paragraph, as being indefinite.

Claim 9 has been amended to overcome the rejection.

Rejections under 35 USC §102(e)

Claims 4-5 are rejected under 35 USC §102(e) as being anticipated by Matsushita (U.S. Patent No. 6,413,810).

The Examiner alleged that Matsushita discloses a “ridge structure (27) made of insulating film material formed on an upper surface of the gate electrode of the second field effect transistor”

The silicon nitride film (27) in Matsuhashi, however, has a rectangular cross-sectional shape, but the film (27) does not have a "ridge structure of insulating film material," which is recited in claim 4 and shown as, for example, "the ridge structure 11" in Fig. 2. Also, Matsuhashi does not show "a first field effect transistor" and "a second field effect transistor" which are different from each other.

Claim 4 has been amended for clarification to recite "a ridge structure made of insulating material formed on an upper surface of the second gate electrode ~~of said second field effect transistor~~ but not on an upper surface of the first gate electrode."

The ridge structure of claim 4 corresponds to the ridge structure 11 shown in Fig. 2. The ridge structure covers the looped region adjacent to the outer periphery of the top surface of the gate electrode 7, but does not cover the inner region surrounded by the looped region. In Matsuhashi, the SiN film 127 covers the all area of the top surface of the gate electrode 126.

For at least these reasons, claim 4 patentably distinguishes over Matsuhashi. Claim 5, depending from claim 4, also patentably distinguish over the cited reference for at least the same reasons.

Moreover, claim 5 further recites "wherein a distance between two portions of said ridge structure extending along a direction crossing a gate length direction is approximately equal to a gate length of said first field effect transistor," which further distinguishes over the prior art. The distance between two portions of the ridge structure extending along a direction crossing a gate length direction corresponds to the width W2 shown in Fig. 1B. Namely, the distance means a gap between the inner periphery lines, which are parallel to each other, of the ridge structure. The gate length of the field effect transistor of claim 5 corresponds to the width W1 shown in Fig. 1A.

New Claim

Claim 11 has been newly added.

The ridge structure made of insulating material formed on an upper surface of the gate electrode is novel regardless the existence of a first field effect transistor. Therefore, new claim 11 reciting the ridge structure has been added.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

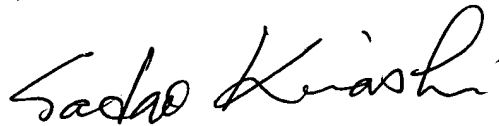
If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

U.S. Patent Application Serial No. 09/996,758

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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IN THE CLAIMS:

Claim 11 has been newly added.

Claims 4, 6 and 9 have been amended as follows:

4. (Amended) A semiconductor device comprising:

a first field effect transistor having a first gate electrode formed on a first section of a semiconductor substrate;

a second field effect transistor having a second gate electrode formed on the second section of said semiconductor substrate; and

a ridge structure made of insulating material formed on an upper surface of the second gate electrode of said second field effect transistor but not on an upper surface of the first gate electrode, said ridge structure extending along side edges of the second gate electrode.

6. (Amended) A semiconductor device according to claim 4, further comprising a metal silicide film covering an upper surface of the first gate electrode of said second field effect transistor excepting the upper surface ~~not~~ formed with said ridge structure.

9. (Amended) A semiconductor device comprising:

a first field effect transistor having a first gate electrode formed on a first section of a semiconductor substrate;

a second field effect transistor having a second gate electrode formed on a second section of said semiconductor substrate;

a first film made of a first material and disposed on the second gate electrode of said second field effect transistor, an outer periphery of said first film being aligned with side edges of the underlying second gate electrode;

a second film disposed on said first film, an outer periphery of said second film positioning inside the outer periphery of said first film, and said second film being made of a second material having an etching resistance different from the first material; and

a third film disposed on the first gate electrode of said first field effect transistor, an outer periphery of said third film being aligned with side edges of the underlying first gate electrode, said third film being made of the second material.